IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1 and 13 in accordance with the following:

1. (Currently Amended) An error detection/correction system in data transmission between a plurality of modules that are connected via buses in a controller, the system comprising:

in each of the modules,

a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity generating an error correction code to be added to data to be transmitted to the bus connected to the module or to a serial transmission line; and

a plurality of error detection/correction circuits corresponding to a respective one of the error detection/correction code generation circuits, wherein an error detection/correction code generation circuit and an error detection/correction circuit are switched over dependent upon a kind, a length, and a timing of the data to be transferred to detect and correct an error of the data having the error correction code added.

2. (Original) The error detection/correction system according to claim 1, wherein the error detection/correction system switches over between error detection/correction codes to be used dependent upon on a phase of transmitting an address, a command, and data.

3. (Original) The error detection/correction system according to claim 1, wherein the error detection/correction system switches over error detection/correction codes to be used dependent upon whether at a time of single access or at a time of burst access.

4. (Original) The error detection/correction system according to claim 1, wherein the error detection/correction system switches over between error detection/correction codes to be used, dependent upon a data quantity to be transferred.

5. (Previously Presented) A controller in which a plurality of modules that adopt the error detection/correction system according to claim 1 are connected via buses.

6. (Previously Presented) The controller according to claim 5, wherein

the controller comprises a serial transfer module that connects a plurality buses connected with the plurality of modules, by means of a serial transmission line, and

a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity, and error detection/correction circuits corresponding to the error detection/correction code generation circuits are built into the serial transfer module, and the error detection/correction system is used for the serial transfer.

7. (Previously Presented) A controller in which a plurality of modules that adopt the error detection/correction system according to claim 2 are connected via buses.

8. (Previously Presented) A controller in which a plurality of modules that adopt the error detection/correction system according to claim 3 are connected via buses.

9. (Previously Presented) A controller in which a plurality of modules that adopt the error detection/correction system according to claim 4 are connected via buses.

10–12. (Cancelled)

13. (Currently Amended) An error detection/correction system, comprising:

a plurality of modules connected via buses to transmit data, each of the modules including,

a plurality of error detection/correction code generation circuits and a plurality of error detection/correction circuits corresponding to a respective one of the error detection/correction code generation circuits, the plurality of error detection/correction code generation circuits generating an error correction code to be added to the data to be transmitted to one of the buses connected to one of the modules, wherein an error detection/correction code generation circuit and an error detection/correction circuit are switched over dependent upon a kind, a length, and a timing of the data to be transferred to detect and correct an error of the data having the error correction code added.